PATENT
Attorney's Docket No. 0023-0135

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:	)	**Mail Stop Appeal Brief - Patents**
	)	
Alok SHARMA	)	Group Art Unit: 2426
	)	
Application No.: 09/800,397	)	Examiner: J. Zhong
	)	
Filed: March 5, 2001	)	
	)	
For: TRANSCEIVER CHANNEL BANK WITH REDUCED CONNECTOR DENSITY	)	

APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief - Patents
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

This Appeal Brief is submitted in response to the final Office Action mailed July 31, 2009 and in support of the Notice of Appeal filed November 2, 2009.

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I. REAL PARTY IN INTEREST

The real party in interest of the present application, solely for purposes of identifying and avoiding potential conflicts of interest by board members due to working in matters in which the member has a financial interest is JUNIPER NETWORKS, INC., which is an assignee of record of the present application.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals, interferences, or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1, 3-10, 12-17, and 22-40 are pending in the present application. Claims 2, 11, and 18-21 were previously canceled without prejudice or disclaimer. Claims 1, 3-10, 12-17, and 22-40 were finally rejected in the final Office Action dated July 31, 2009, and are the subject of the present appeal. Claims 1, 3-10, 12-17, and 22-40 are reproduced in the Claim Appendix of this Appeal Brief.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the final Office Action mailed July 31, 2009.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The following summary of the presently claimed subject matter indicates certain portions of the specification (including the drawings) that provide examples of embodiments of elements of the claimed subject matter. It is to be understood that other portions of the specification not cited herein may also provide examples of embodiments of elements of the claimed subject matter. It is also to

be understood that the indicated examples are merely examples, and the scope of the claimed subject matter includes alternative embodiments and equivalents thereof. References herein to the specification are thus intended to be exemplary and not limiting.

Claim 1 recites: a method for provisioning multiple digital receivers, comprising: providing an analog to digital converter having an analog input and a digital output (*see*, e.g., original claim 1; Fig. 9 (500)); providing a plurality of digital receivers, each receiver having a programmable center frequency (*see*, *e.g.*, original claim 1; Fig. 9 (250); p. 11, lines 19-21), where the plurality of digital receivers are to receive digitized samples from the analog to digital converter and where each of the plurality of digital receivers includes a low-pass digital filter (*see*, *e.g.*, Fig. 9 (500, 250); p. 11, lines 10-12; p. 13, lines 1-3); maintaining pre-computed sets of filter coefficients in non-volatile storage, each set corresponding to one of the plurality of low-pass digital filters, each filter having one of a predetermined set of bandwidths (*see*, *e.g.*, original claim 2; p. 11, lines 10-12); receiving a request to provision a selected one of the plurality of digital receivers (*see*, *e.g.*, p. 13, lines 1-3; Fig. 13 (1350)); selecting a first center frequency and a first bandpass bandwidth for provisioning the selected one of the plurality of digital receivers (*see*, *e.g.*, original claim 2; p. 14, lines 2-4); retrieving the filter coefficients associated with the first bandpass bandwidth (*see*, *e.g.*, original claim 2; p. 13, lines 20-22); subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency (*see*, *e.g.*, original claim 2; p. 14, lines 2-4); and loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers (*see*, *e.g.*, original claim 2; p. 14, lines 4-6).

Claim 5 recites: the method of claim 1, where the analog to digital converter and the plurality of digital receivers are located within the upstream section of a cable modem termination system (CMTS) channel bank organized into upstream and downstream channels (*see*, *e.g.*, original claim 5; Fig. 16).

Claim 6 recites: the method of claim 5, where the ratio of the number of upstream channels demodulated by the CMTS channel bank to a number of upstream input connectors of the CMTS channel bank is M (*see*, *e.g.*, original claim 6; p. 15, lines 12-18).

Claim 7 recites: the method of claim 6, where M is 16 (*see*, *e.g.*, original claim 7; p. 15, lines 12-18).

Claim 8 recites: the method of claim 1, where the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit (*see*, *e.g.*, original claim 8; p. 14, lines 16-18; Fig. 14).

Claim 24 recites: a system for provisioning multiple digital receivers, comprising: an analog to digital converter having an analog input and a digital output (*see*, e.g., original claim 1; Fig. 9 (500)); a plurality of digital receivers, each of the plurality of digital receivers having a programmable center frequency, and each of the plurality of digital receivers including a low-pass digital filter (*see*, *e.g.*, original claim 1; Fig. 9 (250); p. 11, lines 19-21); means for coupling digitized samples to the plurality of digital receivers (*see*, *e.g.*, Fig. 9 (500, 250); p. 11, lines 10-12; p. 13, lines 1-3); means for maintaining pre-computed sets of filter coefficients in non-volatile storage, each set corresponding to one of plurality of low-pass digital filters, each filter having one of a predetermined set of bandwidths (*see*, *e.g.*, original claim 2; p. 11, lines 10-12); means for receiving a request to provision a selected one of the plurality of digital receivers (*see*, *e.g.*, p. 13, lines 1-3; Fig. 13 (1350)); means for selecting a first center frequency and a first bandpass bandwidth for provisioning the selected one of the plurality of digital receivers (*see*, *e.g.*, original claim 2; p. 14, lines 2-4); means for retrieving the filter coefficients associated with the first bandpass bandwidth (*see*, *e.g.*, original claim 2; p. 13, lines 20-22); means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency (*see*, *e.g.*, original claim 2; p.

14, lines 2-4); and means for loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers (*see*, *e.g.*, original claim 2; p. 14, lines 4-6).

Claim 27 recites: the method of claim 24, where the analog to digital converter and the plurality of digital receivers are located within the upstream section of a CMTS channel bank organized into upstream and downstream channels (*see*, *e.g.*, original claim 5; Fig. 16).

Claim 28 recites: the method of claim 27, where the ratio of the number of upstream channels demodulated by the CMTS channel bank to a number of upstream input connectors of the CMTS channel bank is M (*see*, *e.g.*, original claim 6; p. 15, lines 12-18).

Claim 29 recites: the method of claim 28, where M is 16 (*see*, *e.g.*, original claim 7; p. 15, lines 12-18).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 3, 4, 8, 16, 17, 22-26, and 36-40 stand rejected under 35 U.S.C. § 103(a) as unpatentable over BARHAM et al. (U.S. Patent No. 6,721,371) in view of YASUDA et al. (U.S. Patent No. 6,466,913).

B. Claims 5-7, 13, 27-29, and 33 stand rejected under 35 U.S.C. § 103(a) as unpatentable over BARHAM et al. in view of YASUDA et al., and further in view of QUIGLEY et al. (U.S. Patent No. 6,650,624).

C. Claims 14, 15, 34, and 35 stand rejected under 35 U.S.C. § 103(a) as unpatentable over BARHAM et al. in view of YASUDA et al., further in view of QUIGLEY et al., and still further in view of PEYROVIAN (U.S. Patent No. 5,768,682).

D. Claims 9, 10, 12, and 30-32 stand rejected under 35 U.S.C. § 103(a) as unpatentable over BARHAM et al. in view of YASUDA et al., further in view of QUIGLEY et al., and still further in view of Applicant's Fig. 17(A).

VII. ARGUMENTS

A. The rejection of claims 1, 3, 4, 8, 16, 17, 22-26, and 36-40 under 35 U.S.C. § 103(a) as unpatentable over BARHAM et al. in view of YASUDA et al. should be reversed.

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 U.S.P.Q. 173 (C.C.P.A. 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S. Ct. 684, 383 U.S. 1, 148 U.S.P.Q. 459 (1966). KSR International Co. v. Teleflex Inc., 550 U.S. 398, 127 S. Ct. 1727 (2007). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

1. Claims 1, 3, 4, 16, 17, 22, and 23

Claim 1 is directed to a method for provisioning multiple digital receivers. The method includes providing an analog to digital converter having an analog input and a digital output; providing a plurality of digital receivers, each receiver having a programmable center frequency, where the plurality of digital receivers are to receive digitized samples from the analog to digital converter and where each of the plurality of digital receivers includes a low-pass digital filter; maintaining pre-computed sets of filter coefficients in non-volatile storage, each set corresponding to one of the plurality of low-pass digital filters, each filter having one of a predetermined set of bandwidths; receiving a request to provision a selected one of the plurality of digital receivers;

selecting a first center frequency and a first bandpass bandwidth for provisioning the selected one of the plurality of digital receivers; retrieving the filter coefficients associated with the first bandpass bandwidth; subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency; and loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers. BARHAM et al. and YASUDA et al., whether take alone or in any reasonable combination, do not disclose or suggest one or more of these features.

For example, BARHAM et al. and YASUDA et al. do not disclose or suggest subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency. The Examiner appears to admit that BARHAM et al. does not disclose this feature and relies on col. 7, lines 1-9; col. 7, line 50-col. 8, line 18; col. 10, lines 28-47; and col. 11, lines 22-41 of YASUDA et al. as allegedly disclosing this feature (final Office Action, p. 4). Appellant disagrees with the Examiner's interpretation of YASUDA et al.

At col. 7, lines 1-10, YASUDA et al. discloses:

> The ADC 311 inputs an analog right-channel sound signal (R CH INPUT), and converts the input signal into a digital signal. The ADC 311 supplies the digital signal to each of the inputs of the FIR filter 312a and the FIR filter 312b. The coefficient buffer 313a stores filter coefficients of the FIR filter 312a which are read from the coefficient ROM 302 and transmitted by the CPU 301. The coefficient buffer 313b stores filter coefficients of the FIR filter 312b which are read from the coefficient ROM 302 and transmitted by the CPU 301.

This section of YASUDA et al. discloses that filter coefficients are read from a coefficient ROM 302 by a CPU 301 and transmitted to a coefficient buffer 313a. This section of YASUDA et al. in no way discloses or suggests subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 1. In fact, this section of YASUDA et al. does not disclose or suggest subjecting retrieved coefficients to any sort of transformation, let alone a bandpass transformation corresponding to the first center frequency. In YASUDA et al., the

coefficients that are read from the coefficient ROM 302 are merely transmitted to a coefficient buffer 313a – no transformation of these coefficients occurs.

Moreover, Appellant respectfully submits that reading and transmitting filter coefficients are not equivalent to subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 1. Further still, Appellant notes that this section of YASUDA et al. makes no mention of a center frequency at all.

At col. 7, line 50-col. 8, line 19, YASUDA et al. discloses:

> In the above-mentioned system of FIG. 4, the CPU 301 reads filter coefficients of the right-channel FIR filters 312a and 312b from the coefficient ROM 302 in accordance with the localization shift signal, and transmits the filter coefficients to one of the coefficient buffers 313a and 313b alternately. At the same time, the CPU 301 reads filter coefficients of the left-channel FIR filters 322a and 322b from the coefficient ROM 302 in accordance with the localization shift signal, and transmits the filter coefficients to one of the coefficient buffers 323a and 323b alternately. If the FIR filter 312a has already output the localized sound signal based on the previous filter coefficients in the coefficient buffer 313a, the FIR filter 312b outputs the localized sound signal based on the new filter coefficients in the coefficient buffer 313b. The fader 315 serves to make the previous-coefficient-based localization sound signals to fade out within a cross-fade period and to simultaneously make the new-coefficient-based localization sound signals to fade in within the cross-fade period. Similarly, if the FIR filter 322a has already output the localized sound signal based on the previous filter coefficients in the coefficient buffer 323a, the FIR filter 322b outputs the localized sound signal based on the new filter coefficients in the coefficient buffer 323b. The fader 325 serves to make the previous-coefficient-based localization sound signals to fade out within the cross-fade period and to simultaneously make the new-coefficient-based localization sound signals to fade in within the cross-fade period.

This section of YASUDA et al. discloses that filter coefficients are read from a coefficient ROM 302 in accordance with a localization shift signal by a CPU 301 and transmitted to coefficient buffers 322a, 322b, 323a and 323b. This section of YASUDA et al. in no way discloses or suggests subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 1. In fact, like the previously cited section of YASUDA et al., this section of YASUDA et al. does not disclose or suggest subjecting retrieved coefficients to any sort of transformation, let alone a bandpass transformation corresponding to the first center

frequency. In YASUDA et al., the coefficients that are read from the coefficient ROM 302 are merely transmitted to a coefficient buffer 313a – no transformation of these coefficients occurs.

Moreover, Appellant respectfully submits that reading and transmitting filter coefficients are not equivalent to subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 1. Further still, Appellant notes that this section of YASUDA et al. makes no mention of a center frequency at all.

At col. 10, lines 28-47, YASUDA et al. discloses:

> In the system control module 1 of FIG. 7, the initial parameter generating unit 34 generates initial parameters to be stored in the initial parameter memory 35. The initial parameter memory 35 stores a plurality of sets of initial parameters with respect to a plurality of predetermined direction angles about the front position of the listener. The CPU 31 reads one of the sets of initial parameters from the initial parameter memory 35 in accordance with the localization shift signal, and transmits the initial parameters to the optimum parameter calculating unit 36. The optimum parameter calculating unit 36 calculates an optimum filter parameter based on the initial parameters transmitted by the CPU 31. The filter coefficient determining unit 37 determines filter coefficients of each of the S/L filter 12 and the S/L filter 22 based on the optimum filter parameter supplied by the optimum parameter calculating unit 36. The CPU 31 controls the filter coefficient determining unit 37 such that the determined filter coefficients are supplied from the filter coefficient determining unit 37 to each of the coefficient buffer 13 and the coefficient buffer 23.

This section of YASUDA et al. is directed to calculating a filter parameter based on initial parameters. YASUDA et al. appears to disclose that the initial parameters relate to direction angles. This section of YASUDA et al. does not mention subjecting any retrieved coefficients to any transformation, let alone a bandpass transformation corresponding to the first center frequency, as recited in claim 1. Further still, Appellant notes that this section of YASUDA et al. makes no mention of a center frequency at all.

At col. 11, lines 22-41, YASUDA et al. discloses:

> As previously described, one of the sets of initial parameters (fc, Q, L) (which are relevant to the localization shift signal) is read from the initial parameter memory 35 by the CPU 31, and the CPU 31 transmits the initial parameters to the optimum parameter calculating unit 36. The optimum parameter calculating unit 36 calculates

> an optimum filter parameter based on the initial parameters transmitted by the CPU 31. The filter coefficient determining unit 37 determines filter coefficients of each of the S/L filter 12 and the S/L filter 22 based on the optimum filter parameter supplied by the optimum parameter calculating unit 36. The CPU 31 controls the filter coefficient determining unit 37 such that the determined filter coefficients are supplied from the filter coefficient determining unit 37 to each of the coefficient buffer 13 and the coefficient buffer 23. Hence, the S/L filters 12 and 13 in the sound localization control system provide the right-channel and left-channel output signals at their outputs which suit the localization shift signal at the input of the CPU 31.

This section of YASUDA et al. discloses that initial parameters are read from a memory, and then an optimum parameter calculating unit calculates an optimum filter based on the initial parameters. This section of YASUDA et al. does not disclose subjecting retrieved filter coefficients to a bandpass transformation, as recited in claim 1. Instead, this section of YASUDA et al. discloses determining a filter coefficient based on initial parameters. As such, this section of YASUDA et al. cannot reasonably be construed to disclose or suggest subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 1.

Appellant notes that, in essence, the Examiner alleges that a CPU 301 selecting a filter coefficient and setting the function of a FIR filter using that filter coefficient are the equivalent of subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 1. Appellant respectfully submits that the Examiner's allegation completely omits (i.e., does not address) the claimed feature, subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, and renders moot the Examiner's allegation regarding another claimed feature, loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers.

Appellant respectfully submits that merely "selecting" a filter coefficient and "setting" a function of a FIR filter, as alleged by the Examiner, do not disclose or suggest subjecting the retrieved coefficients to a bandpass transformation. Subjecting a retrieved coefficient to a bandpass transformation, as recited in claim 1 involves more than merely "selecting" the coefficient. Claim 1

recites that a retrieved coefficient is subjected to a bandpass transformation – a feature that is neither addressed by the Examiner, nor disclosed or suggested by YASUDA et al.

Furthermore, Appellant respectfully submits that the Examiner's allegation with regard to the above feature renders moot the Examiner's allegation that YASUDA et al. discloses loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers. The Examiner's allegation with regard to both of these features includes transmitting coefficients to coefficient buffers (*see* final Office Action, p. 4). Specifically, the Examiner cites col. 7, lines 1-9, 50-67 of YASUDA et al. as disclosing both of these features.

As discussed above, this section of YASUDA et al. discloses that filter coefficients are read from a coefficient ROM 302 in accordance with a localization shift signal by a CPU 301 and transmitted to coefficient buffers 322a, 322b, 323a and 323b. Therefore, Appellant respectfully submits that the Examiner's allegation with regard to one feature, subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, renders moot the Examiner's allegation with regard to the other feature, loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers, as recited in claim 1. As such, Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness with respect to claim 1.

Since BARHAM et al. and YASUDA et al. do not disclose or suggest subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, BARHAM et al. and YASUDA et al., whether taken alone or in any reasonable combination, cannot disclose or suggest loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers, as also recited in claim 1.

Therefore, the alleged combination of BARHAM et al. and YASUDA et al. could not fairly be construed to disclose the above-mentioned feature of claim 1. Furthermore, Appellant asserts that

the reasons for combining BARHAM et al. and YASUDA et al. do not satisfy the requirements of 35 U.S.C. § 103.

For example, with respect to the reasons for combining BARHAM et al. with YASUDA et al., the Examiner alleges (final Office Action, pp. 4-5):

> [I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to have coefficients storage as taught by Yasuda to the FIR filter of Barham in order to provide an FIR filter that is capable filtering variety of frequency ranges by change the coefficients, without change the hardware.

Appellant submits that the Examiner's allegation is merely a conclusory statement of an alleged benefit of the combination. Such conclusory statements have been repeatedly held to be insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon KSR International Co. v. Teleflex Inc., 550 U.S. 398, 82 U.S.P.Q.2d 1385 (2007) (citing In re Kahn, 441 F.3d 977, 988, 78 U.S.P.Q.2d 1329 (Fed. Cir. 2006)), where it was held that rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

Furthermore, the Examiner does not explain how combining YASUDA et al.'s alleged coefficient storage with BARHAM et al.'s alleged FIR filter would provide the alleged benefit. Therefore, the Examiner's allegations fall short of providing the articulated reasoning required by KSR.

For at least the foregoing reasons, Appellant submits that the rejection of claim 1 under 35 U.S.C. § 103(a) based on YASUDA et al. and BARHAM et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

Claims 3, 4, 16, 17, 22, and 23 depend from claim 1. Therefore, Appellant requests that the rejection of these claims be reversed for at least the reasons given above with respect to claim 1.

2. Claim 8

Claim 8 recites that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit. YASUDA et al. and BARHAM et al., whether taken alone or in combination, do not disclose or suggest the above feature of claim 8.

The Examiner relies on col. 3, lines 53-55, col. 4, lines 45-50, and col. 5, lines 49-57 of BARHAM et al. as allegedly disclosing "wherein the analog to digital converter, the plurality of digital receivers, and storage (e.g., registers or memory) are implemented on a single integrated circuit (e.g., bank or array of IC demodulators 10)" (final Office Action, p. 7). The Examiner also relies on YASUDA et al. for allegedly disclosing "non-volatile storage (e.g., ROM 202, 302; Fig. 4)" (final Office Action, p. 7). Appellant disagrees with the Examiner's interpretation of YASUDA et al. and BARHAM et al.

At col. 3, lines 51-55, BARHAM et al. discloses:

> The high rate demodulation system consists of a high rate analog to digital converter 102 and demultiplexer 103, bank or array of IC demodulators 10 where one of the demodulators is designated as the master or first demodulator 10A, a phase reference interface 105, a timing interface 106, and a data processor 104.

This section of BARHAM et al. discloses various components of a high rate demodulation system. The high rate demodulation system of BARHAM et al. includes, *inter alia*, a bank or array of IC demodulators 10. The Examiner appears to allege that the bank or array of IC demodulators, disclosed by BARHAM et al., corresponds to the analog to digital converter, the plurality of digital receivers, and storage (which are implemented on a single integrated circuit), as recited in claim 8. Appellant respectfully submits that this section of BARHAM et al. provides no support whatsoever for the Examiner's allegation. In fact, this section of BARHAM et al. makes no mention of storage at all.

Moreover, the Examiner's interpretation is inconsistent with the disclosure of BARHAM et al. BARHAM et al. discloses, *inter alia*, a high rate analog to digital converter 102 and a bank or array of IC demodulators 10. As illustrated by Fig. 18 of BARHAM et al., the demodulators 10 appear to each be implemented as a separate IC. In fact, in Fig., 18 of BARHAM et al., each demodulator 10 is labeled as a "demodulator ASIC [Application Specific Integrated Circuit]." Fig. 18 of BARHAM et al. further illustrates that analog to digital converter 102 is separate from the demodulator ASICs 10. Thus, Appellant respectfully submits that BARHAM et al. does not disclose or suggest, even under the Examiner's interpretation, that the high rate analog to digital converter 102 and bank or array of IC demodulators 10 are implemented on a single integrated circuit. Therefore, this section of BARHAM et al. cannot reasonably be construed as disclosing or suggesting that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit, as recited in claim 8.

At col. 4, lines 45-50, BARHAM et al. discloses:

> By linking within each RADIS 10, the coherent processor and the weight processor components with the coherent memory, and by providing a wide configurability through a programmable input port, a high rate demodulator system is made available for various digital data reception applications.

This section of BARHAM et al. has nothing to do with the above-mentioned feature of claim 8. Furthermore, as discussed above, a RADIS 10 (previously referred to by BARHAM et al. as an "IC demodulator" or a "demodulator ASIC") does not disclose or suggest that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit, as recited in claim 8.

At col. col. 5, lines 49-57, BARHAM et al. discloses:

> Each RADIS 10 includes a front end 12 that generally performs DC removal, phase shifting, accumulation and down-sampling of the input IQ signals. The output of the front end 12 is applied to a reconfigurable FIR filter 14. The FIR filter 14, in the presently preferred embodiment of this invention, has 64 stages implemented with 32

> 1-bit taps. A set of registers forming a weight stack or ring 16 (8x34) is connected to the parallel input port for being programmed from the external processor (not shown).

This section of BARHAM et al. describes a front end 12 of a RADIS 10 (previously referred to by BARHAM et al. as an "IC demodulator" or a "demodulator ASIC"). As discussed above, a RADIS 10 does not disclose or suggest that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit, as recited in claim 8.

At Fig. 4, YASUDA et al. illustrates a sound localization control system having a cross-fade function (YASUDA et al., col. 5, lines 5-6). This system includes a coefficient ROM 302. Without acquiescing in the Examiner's interpretation that this coefficient ROM 302 corresponds to the non-volatile storage, recited in claim 8, this section of YASUDA et al. is completely silent with regard to integrated circuits. Thus, this section of YASUDA et al. cannot disclose or suggest that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit, as recited in claim 8.

For at least the foregoing additional reasons, Appellant submits that the rejection of claim 8 under 35 U.S.C. § 103(a) based on YASUDA et al. and BARHAM et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

3. Claims 24-26 and 37-40

Claim 24 is directed to a system for provisioning multiple digital receivers, comprising an analog to digital converter having an analog input and a digital output; a plurality of digital receivers, each of the plurality of digital receivers having a programmable center frequency, and each of the plurality of digital receivers including a low-pass digital filter; means for coupling digitized samples to the plurality of digital receivers; means for maintaining pre-computed sets of filter coefficients in non-volatile storage, each set corresponding to one of plurality of low-pass

digital filters, each filter having one of a predetermined set of bandwidths; means for receiving a request to provision a selected one of the plurality of digital receivers; means for selecting a first center frequency and a first bandpass bandwidth for provisioning the selected one of the plurality of digital receivers; means for retrieving the filter coefficients associated with the first bandpass bandwidth; means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency; and means for loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers. BARHAM et al. and YASUDA et al., whether take alone or in any reasonable combination, do not disclose or suggest one or more of these features.

For example, BARHAM et al. and YASUDA et al. do not disclose or suggest means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency. The Examiner appears to admit that BARHAM et al. does not disclose this feature and relies on col. 7, lines 1-9; col. 7, line 50-col. 8, line 18; col. 10, lines 28-47; and col. 11, lines 22-41 of YASUDA et al. as allegedly disclosing this feature (final Office Action, pp. 4, 8). Appellant disagrees with the Examiner's interpretation of YASUDA et al.

At col. 7, lines 1-10, YASUDA et al. discloses:

> The ADC 311 inputs an analog right-channel sound signal (R CH INPUT), and converts the input signal into a digital signal. The ADC 311 supplies the digital signal to each of the inputs of the FIR filter 312a and the FIR filter 312b. The coefficient buffer 313a stores filter coefficients of the FIR filter 312a which are read from the coefficient ROM 302 and transmitted by the CPU 301. The coefficient buffer 313b stores filter coefficients of the FIR filter 312b which are read from the coefficient ROM 302 and transmitted by the CPU 301.

This section of YASUDA et al. discloses that filter coefficients are read from a coefficient ROM 302 by a CPU 301 and transmitted to a coefficient buffer 313a. This section of YASUDA et al. in no way discloses or suggests means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 24. In fact, this

section of YASUDA et al. does not disclose or suggest means for subjecting retrieved coefficients to any sort of transformation, let alone a bandpass transformation corresponding to the first center frequency. In YASUDA et al., the coefficients that are read from the coefficient ROM 302 are merely transmitted to a coefficient buffer 313a – no transformation of these coefficients occurs.

Moreover, Appellant respectfully submits that reading and transmitting filter coefficients are not equivalent to means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 24. Further still, Appellant notes that this section of YASUDA et al. makes no mention of a center frequency at all.

At col. 7, line 50-col. 8, line 19, YASUDA et al. discloses:

> In the above-mentioned system of FIG. 4, the CPU 301 reads filter coefficients of the right-channel FIR filters 312a and 312b from the coefficient ROM 302 in accordance with the localization shift signal, and transmits the filter coefficients to one of the coefficient buffers 313a and 313b alternately. At the same time, the CPU 301 reads filter coefficients of the left-channel FIR filters 322a and 322b from the coefficient ROM 302 in accordance with the localization shift signal, and transmits the filter coefficients to one of the coefficient buffers 323a and 323b alternately. If the FIR filter 312a has already output the localized sound signal based on the previous filter coefficients in the coefficient buffer 313a, the FIR filter 312b outputs the localized sound signal based on the new filter coefficients in the coefficient buffer 313b. The fader 315 serves to make the previous-coefficient-based localization sound signals to fade out within a cross-fade period and to simultaneously make the new-coefficient-based localization sound signals to fade in within the cross-fade period. Similarly, if the FIR filter 322a has already output the localized sound signal based on the previous filter coefficients in the coefficient buffer 323a, the FIR filter 322b outputs the localized sound signal based on the new filter coefficients in the coefficient buffer 323b. The fader 325 serves to make the previous-coefficient-based localization sound signals to fade out within the cross-fade period and to simultaneously make the new-coefficient-based localization sound signals to fade in within the cross-fade period.

This section of YASUDA et al. discloses that filter coefficients are read from a coefficient ROM 302 in accordance with a localization shift signal by a CPU 301 and transmitted to coefficient buffers 322a, 322b, 323a and 323b. This section of YASUDA et al. in no way discloses or suggests means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 24. In fact, like the previously cited section of YASUDA et al.,

this section of YASUDA et al. does not disclose or suggest means for subjecting retrieved coefficients to any sort of transformation, let alone a bandpass transformation corresponding to the first center frequency. In YASUDA et al., the coefficients that are read from the coefficient ROM 302 are merely transmitted to a coefficient buffer 313a – no transformation of these coefficients occurs.

Moreover, Appellant respectfully submits that reading and transmitting filter coefficients are not equivalent to means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 24. Further still, Appellant notes that this section of YASUDA et al. makes no mention of a center frequency at all.

At col. 10, lines 28-47, YASUDA et al. discloses:

> In the system control module 1 of FIG. 7, the initial parameter generating unit 34 generates initial parameters to be stored in the initial parameter memory 35. The initial parameter memory 35 stores a plurality of sets of initial parameters with respect to a plurality of predetermined direction angles about the front position of the listener. The CPU 31 reads one of the sets of initial parameters from the initial parameter memory 35 in accordance with the localization shift signal, and transmits the initial parameters to the optimum parameter calculating unit 36. The optimum parameter calculating unit 36 calculates an optimum filter parameter based on the initial parameters transmitted by the CPU 31. The filter coefficient determining unit 37 determines filter coefficients of each of the S/L filter 12 and the S/L filter 22 based on the optimum filter parameter supplied by the optimum parameter calculating unit 36. The CPU 31 controls the filter coefficient determining unit 37 such that the determined filter coefficients are supplied from the filter coefficient determining unit 37 to each of the coefficient buffer 13 and the coefficient buffer 23.

This section of YASUDA et al. is directed to calculating a filter parameter based on initial parameters. YASUDA et al. appears to disclose that the initial parameters relate to direction angles. This section of YASUDA et al. does not mention means for subjecting any retrieved coefficients to any transformation, let alone a bandpass transformation corresponding to the first center frequency, as recited in claim 24. Further still, Appellant notes that this section of YASUDA et al. makes no mention of a center frequency at all.

At col. 11, lines 22-41, YASUDA et al. discloses:

> As previously described, one of the sets of initial parameters (fc, Q, L) (which are relevant to the localization shift signal) is read from the initial parameter memory 35 by the CPU 31, and the CPU 31 transmits the initial parameters to the optimum parameter calculating unit 36. The optimum parameter calculating unit 36 calculates an optimum filter parameter based on the initial parameters transmitted by the CPU 31. The filter coefficient determining unit 37 determines filter coefficients of each of the S/L filter 12 and the S/L filter 22 based on the optimum filter parameter supplied by the optimum parameter calculating unit 36. The CPU 31 controls the filter coefficient determining unit 37 such that the determined filter coefficients are supplied from the filter coefficient determining unit 37 to each of the coefficient buffer 13 and the coefficient buffer 23. Hence, the S/L filters 12 and 13 in the sound localization control system provide the right-channel and left-channel output signals at their outputs which suit the localization shift signal at the input of the CPU 31.

This section of YASUDA et al. discloses that initial parameters are read from a memory, and then an optimum parameter calculating unit calculates an optimum filter based on the initial parameters. This section of YASUDA et al. does not disclose means for subjecting retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 24. Instead, this section of YASUDA et al. discloses determining a filter coefficient based on initial parameters. As such, this section of YASUDA et al. cannot reasonably be construed to disclose or suggest means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 24.

Appellant notes that, in essence, the Examiner alleges that a CPU 301 selecting a filter coefficient and setting the function of a FIR filter using that filter coefficient are the equivalent of means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, as recited in claim 24. Appellant respectfully submits that the Examiner's allegation completely omits (i.e., does not address) the claimed feature, means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, and renders moot the Examiner's allegation regarding another claimed feature, means for loading the

transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers.

Appellant respectfully submits that merely "selecting" a filter coefficient and "setting" a function of a FIR filter, as alleged by the Examiner, do not disclose or suggest means for subjecting the retrieved coefficients to a bandpass transformation corresponding to the first center frequency. Means for subjecting a retrieved coefficient to a bandpass transformation, as recited in claim 24, involves more than merely "selecting" the coefficient. Claim 24 recites that a retrieved coefficient is subjected to a bandpass transformation – a feature that is neither addressed by the Examiner, nor disclosed or suggested by YASUDA et al.

Furthermore, Appellant respectfully submits that the Examiner's allegation with regard to the above feature renders moot the Examiner's allegation that YASUDA et al. discloses means for loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers. The Examiner's allegation with regard to both of these features includes transmitting coefficients to coefficient buffer (*see* final Office Action, p. 4). Specifically, the Examiner cites col. 7, lines 1-9, 50-67 of YASUDA et al. as disclosing both of these features.

As discussed above, this section of YASUDA et al. discloses that filter coefficients are read from a coefficient ROM 302 in accordance with a localization shift signal by a CPU 301 and transmitted to coefficient buffers 322a, 322b, 323a and 323b. Therefore, Appellant respectfully submits that the Examiner's allegation with regard to one feature, means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, renders moot the Examiner's allegation with regard to the other feature, means for loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers, as recited in claim 24. As such, Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness with respect to claim 24.

Since BARHAM et al. and YASUDA et al. do not disclose or suggest means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency, BARHAM et al. and YASUDA et al., whether taken alone or in any reasonable combination, cannot disclose or suggest means for loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers, as also recited in claim 24.

Therefore, the alleged combination of BARHAM et al. and YASUDA et al. could not fairly be construed to disclose the above-mentioned feature of claim 24. Furthermore, Appellant asserts that the reasons for combining BARHAM et al. and YASUDA et al. do not satisfy the requirements of 35 U.S.C. § 103.

For example, with respect to the reasons for combining BARHAM et al. with YASUDA et al., the Examiner alleges (final Office Action, pp. 4-5):

> [I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to have coefficients storage as taught by Yasuda to the FIR filter of Barham in order to provide an FIR filter that is capable filtering variety of frequency ranges by change the coefficients, without change the hardware.

Appellant submits that the Examiner's allegation is merely a conclusory statement of an alleged benefit of the combination. Such conclusory statements have been repeatedly held to be insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon KSR International Co. v. Teleflex Inc., 550 U.S. 398, 82 U.S.P.Q.2d 1385, (2007) (citing In re Kahn, 441 F.3d 977, 988, 78 U.S.P.Q.2d 1329 (Fed. Cir. 2006)), where it was held that rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

Furthermore, the Examiner does not explain how combining YASUDA et al.'s alleged coefficient storage with BARHAM et al.'s alleged FIR filter would provide the alleged benefit.

Therefore, the Examiner's allegations fall short of providing the articulated reasoning required by KSR.

For at least the foregoing reasons, Appellant submits that the rejection of claim 24 under 35 U.S.C. § 103(a) based on YASUDA et al. and BARHAM et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

Claims 25, 26, and 36-40 depend from claim 24. Therefore, Appellant requests that the rejection of these claims be reversed for at least the reasons given above with respect to claim 24.

4. Claim 36

Claim 36 recites that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit. YASUDA et al. and BARHAM et al., whether taken alone or in combination, do not disclose or suggest the above feature of claim 36.

The Examiner relies on col. 3, lines 53-55, col. 4, lines 45-50, and col. 5, lines 49-57 of BARHAM et al. as allegedly disclosing "wherein the analog to digital converter, the plurality of digital receivers, and storage (e.g., registers or memory) are implemented on a single integrated circuit (e.g., bank or array of IC demodulators 10)" (final Office Action, pp. 7, 8). The Examiner also relies on YASUDA et al. for allegedly disclosing "non-volatile storage (e.g., ROM 202, 302; Fig. 4)" (final Office Action, p. 7). Appellant disagrees with the Examiner's interpretation of YASUDA et al. and BARHAM et al.

At col. 3, lines 51-55, BARHAM et al. discloses:

> The high rate demodulation system consists of a high rate analog to digital converter 102 and demultiplexer 103, bank or array of IC demodulators 10 where one of the demodulators is designated as the master or first demodulator 10A, a phase reference interface 105, a timing interface 106, and a data processor 104.

This section of BARHAM et al. discloses that various components of a high rate demodulation system. The high rate demodulation system of BARHAM et al. includes, *inter alia*, a bank or array of IC demodulators 10. The Examiner appears to allege that the bank or array of IC demodulators, disclosed by BARHAM et al., corresponds to the analog to digital converter, the plurality of digital receivers, and storage (which are implemented on a single integrated circuit), as recited in claim 36. Appellant respectfully submits that this section of BARHAM et al. provides no support whatsoever for the Examiner's allegation. In fact, this section of BARHAM et al. makes no mention of storage at all.

Moreover, the Examiner's interpretation is inconsistent with the disclosure of BARHAM et al. BARHAM et al. discloses, *inter alia*, a high rate analog to digital converter 102 and a bank or array of IC demodulators 10. As illustrated by Fig. 18 of BARHAM et al., the demodulators 10 appear to each be implemented as a separate IC. In fact, in Fig., 18 of BARHAM et al., each demodulator 10 is labeled as a "demodulator ASIC [Application Specific Integrated Circuit]." Fig. 18 of BARHAM et al. further illustrates that analog to digital converter 102 is separate from the demodulator ASICs 10. Thus, Appellant respectfully submits that BARHAM et al. does not disclose or suggest, even under the Examiner's interpretation, that the high rate analog to digital converter 102 and bank or array of IC demodulators 10 are implemented on a single integrated circuit. Therefore, this section of BARHAM et al. cannot reasonably be construed as disclosing or suggesting that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit, as recited in claim 36.

At col. 4, lines 45-50, BARHAM et al. discloses:

> By linking within each RADIS 10, the coherent processor and the weight processor components with the coherent memory, and by providing a wide configurability through a programmable input port, a high rate demodulator system is made available for various digital data reception applications.

This section of BARHAM et al. has nothing to do with the above-mentioned feature of claim 36. Furthermore, as discussed above, a RADIS 10 (previously referred to by BARHAM et al. as an "IC demodulator" or a "demodulator ASIC") does not disclose or suggest that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit, as recited in claim 36.

At col. col. 5, lines 49-57, BARHAM et al. discloses:

> Each RADIS 10 includes a front end 12 that generally performs DC removal, phase shifting, accumulation and down-sampling of the input IQ signals. The output of the front end 12 is applied to a reconfigurable FIR filter 14. The FIR filter 14, in the presently preferred embodiment of this invention, has 64 stages implemented with 32 1-bit taps. A set of registers forming a weight stack or ring 16 (8x34) is connected to the parallel input port for being programmed from the external processor (not shown).

This section of BARHAM et al. describes a front end 12 of a RADIS 10 (previously referred to by BARHAM et al. as an "IC demodulator" or a "demodulator ASIC"). As discussed above, a RADIS 10 does not disclose or suggest that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit, as recited in claim 36.

At Fig. 4, YASUDA et al. illustrates a sound localization control system having a cross-fade function (YASUDA et al., col. 5, lines 5-6). This system includes a coefficient ROM 302. Without acquiescing in the Examiner's interpretation that this coefficient ROM 302 corresponds to the non-volatile storage, recited in claim 36, this section of YASUDA et al. is completely silent with regard to integrated circuits. Thus, this section of YASUDA et al. cannot disclose or suggest that the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit, as recited in claim 36.

For at least the foregoing additional reasons, Appellant submits that the rejection of claim 36 under 35 U.S.C. § 103(a) based on YASUDA et al. and BARHAM et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

B. The rejection of claims 5-7, 13, 27-29, and 33 under 35 U.S.C. § 103(a) as unpatentable over BARHAM et al. in view of YASUDA et al., and further in view of QUIGLEY et al. should be reversed.

1. Claims 5, 6 and 13

Claims 5, 6, and 13 depend from claim 1. Without acquiescing in the rejection of claims 5, 6, and 13, the disclosure of QUIGLEY et al. does not remedy the deficiencies in the disclosures of BARHAM et al. and YASUDA et al. set forth above with respect to claim 1. Therefore, BARHAM et al., YASUDA et al., and QUIGLEY et al., whether taken alone or in any reasonable combination, do not disclose or suggest the features recited in claims 5, 6, and 13. For at least the foregoing reasons, Appellant submits that the rejection of claims 5, 6, and 13 under 35 U.S.C. § 103(a) based on BARHAM et al., YASUDA et al., and QUIGLEY et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

2. Claim 7

Claim 7 depends from claim 1. Without acquiescing in the rejection of claim 7, the disclosure of QUIGLEY et al. does not remedy the deficiencies in the disclosures of BARHAM et al. and YASUDA et al. set forth above with respect to claim 1. Therefore, BARHAM et al., YASUDA et al., and QUIGLEY et al., whether taken alone or in any reasonable combination, do not disclose or suggest the features recited in claim 7.

Furthermore, claim 7 recites that the ratio of the number of upstream channels demodulated by the CMTS channel bank to a number of upstream input connectors of the CMTS channel bank is

M, where M is 16. BARHAM et al., YASUDA et al., and QUIGLEY et al., whether taken alone or in any reasonable combination, do not disclose or suggest the above feature of claim 7.

The Examiner alleges that the above feature is merely a matter of design choice. Appellant respectfully disagrees with the Examiner's allegation that the above feature is merely a matter of design choice. Moreover, in accordance with the Examiner's duty to establish a *prima facie* case of obviousness, the Examiner has not presented any evidence to support the Examiner's allegation that the above feature of claim 7 is merely a matter of design choice.

In fact, Appellant respectfully submits that it is not merely a matter of design choice to for the ratio of the number of upstream channels demodulated by the CMTS channel bank to a number of upstream input connectors of the CMTS channel bank to be M, where M is 16, as recited in claim 7. For instance, as described in Appellant's Specification at p. 5, lines 21-24 and p. 6, lines 10-11, "In prior art channel bank systems, every upstream channel requires a respective splitter tap, receiver input including a bulkhead-mount connector, and cabling between the splitter tap and the receiver input. . . . What is needed is a receiver channel bank architecture that permits miniaturization of line cards and channel banks by reducing the number of connectors required." Thus, Appellant respectfully submits that the above feature of claim 7 is not merely a design choice, as alleged by the Examiner. For at least this reason, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claim 7.

Therefore, the alleged combination of BARHAM et al., YASUDA et al., and QUIGLEY et al. could not fairly be construed to disclose the above-mentioned feature of claim 7. Furthermore, Appellant asserts that the reasons for combining BARHAM et al., YASUDA et al., and QUIGLEY et al. do not satisfy the requirements of 35 U.S.C. § 103.

For example, with respect to the reasons for combining QUIGLEY et al. with BARHAM et al. and YASUDA et al., the Examiner alleges (final Office Action, p. 9) (citation omitted):

> [I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to have the CMTS as taught by Quigley to the FIR filter of Barham as modified by Yasuda in order to enhance the data date and/or reliability of upstream communications.

Appellant submits that the Examiner's allegation is merely a conclusory statement of an alleged benefit of the combination. Such conclusory statements have been repeatedly held to be insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon KSR, 550 U.S. at 398, 82 U.S.P.Q.2d at 1385 (citing In re Kahn, 441 F.3d at 988, 78 U.S.P.Q.2d at 1329), where it was held that rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

Furthermore, the Examiner does not explain how combining QUIGLEY et al.'s alleged CMTS with YASUDA et al. and BARHAM et al.'s alleged modified FIR filter would provide the benefit set forth by the Examiner. Therefore, the Examiner's allegations fall short of providing the articulated reasoning required by KSR.

For at least the foregoing additional reasons, Appellant submits that the rejection of claim 7 under 35 U.S.C. § 103(a) based on YASUDA et al., BARHAM et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

3. Claims 27, 28, and 33

Claims 27, 28, and 33 depend from claim 24. Without acquiescing in the rejection of claims 27, 28, and 33, the disclosure of QUIGLEY et al. does not remedy the deficiencies in the disclosures of BARHAM et al. and YASUDA et al. set forth above with respect to claim 24. Therefore, BARHAM et al., YASUDA et al., and QUIGLEY et al., whether taken alone or in any reasonable combination, do not disclose or suggest the features recited in claims 27, 28, and 33. For at least the foregoing reasons, Appellant submits that the rejection of claims 27, 28, and 33 under 35 U.S.C.

§ 103(a) based on BARHAM et al., YASUDA et al., and QUIGLEY et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

4. Claim 29

Claim 29 depends from claim 24. Without acquiescing in the rejection of claim 29, the disclosure of QUIGLEY et al. does not remedy the deficiencies in the disclosures of BARHAM et al. and YASUDA et al. set forth above with respect to claim 24. Therefore, BARHAM et al., YASUDA et al., and QUIGLEY et al., whether taken alone or in any reasonable combination, do not disclose or suggest the features recited in claim 29.

Furthermore, claim 29 recites that the ratio of the number of upstream channels demodulated by the CMTS channel bank to a number of upstream input connectors of the CMTS channel bank is M, where M is 16. BARHAM et al., YASUDA et al., and QUIGLEY et al., whether taken alone or in any reasonable combination, do not disclose or suggest the above feature of claim 29.

The Examiner alleges that the above feature is merely a matter of design choice. Appellant respectfully disagrees with the Examiner's allegation that the above feature is merely a matter of design choice. Moreover, in accordance with the Examiner's duty to establish a *prima facie* case of obviousness, the Examiner has not presented any evidence to support the Examiner's allegation that the above feature of claim 29 is merely a matter of design choice.

In fact, Appellant respectfully submits that it is not merely a matter of design choice to for the ratio of the number of upstream channels demodulated by the CMTS channel bank to a number of upstream input connectors of the CMTS channel bank to be M, where M is 16, as recited in claim 29. For instance, as described in Appellant's Specification at p. 5, lines 21-24 and p. 6, lines 10-11, "In prior art channel bank systems, every upstream channel requires a respective splitter tap, receiver input including a bulkhead-mount connector, and cabling between the splitter tap and the receiver input. . . . What is needed is a receiver channel bank architecture that permits miniaturization of line

cards and channel banks by reducing the number of connectors required." Thus, Appellant respectfully submits that the above feature of claim 29 is not merely a design choice, as alleged by the Examiner. For at least this reason, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claim 29.

Therefore, the alleged combination of BARHAM et al., YASUDA et al., and QUIGLEY et al. could not fairly be construed to disclose the above-mentioned feature of claim 29. Furthermore, Appellant asserts that the reasons for combining BARHAM et al., YASUDA et al., and QUIGLEY et al. do not satisfy the requirements of 35 U.S.C. § 103.

For example, with respect to the reasons for combining QUIGLEY et al. with BARHAM et al. and YASUDA et al., the Examiner alleges (final Office Action, p. 9) (citation omitted):

> [I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to have the CMTS as taught by Quigley to the FIR filter of Barham as modified by Yasuda in order to enhance the data date and/or reliability of upstream communications.

Appellant submits that the Examiner's allegation is merely a conclusory statement of an alleged benefit of the combination. Such conclusory statements have been repeatedly held to be insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon KSR, 550 U.S. at 398, 82 U.S.P.Q.2d at 1385 (citing In re Kahn, 441 F.3d at 988, 78 U.S.P.Q.2d at 1329), where it was held that rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

Furthermore, the Examiner does not explain how combining QUIGLEY et al.'s alleged CMTS with YASUDA et al. and BARHAM et al.'s alleged modified FIR filter would provide the benefit set forth by the Examiner. Therefore, the Examiner's allegations fall short of providing the articulated reasoning required by KSR.

For at least the foregoing additional reasons, Appellant submits that the rejection of claim 29 under 35 U.S.C. § 103(a) based on YASUDA et al., BARHAM et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

C. The rejection of claims 14, 15, 34, and 35 under 35 U.S.C. § 103(a) as unpatentable over BARHAM et al. in view of YASUDA et al., further in view of QUIGLEY et al., and still further in view of PEYROVIAN should be reversed.

1. Claims 14 and 15

Claims 14 and 15 depend from claim 1. Without acquiescing in the rejection of claims 14 and 15, the disclosure of PEYROVIAN does not remedy the deficiencies in the disclosures of BARHAM et al., YASUDA et al., and QUIGLEY et al. set forth above with respect to claim 1. Therefore, BARHAM et al., YASUDA et al., QUIGLEY et al., and PEYROVIAN, whether taken alone or in any reasonable combination, do not disclose or suggest the features recited in claims 14 and 15. For at least the foregoing reasons, Appellant submits that the rejection of claims 14 and 15 under 35 U.S.C. § 103(a) based on BARHAM et al., YASUDA et al., QUIGLEY et al., and PEYROVIAN is improper. Accordingly, Appellant requests that the rejection be reversed.

2. Claims 34 and 35

Claims 34 and 35 depend from claim 24. Without acquiescing in the rejection of claims 34 and 35, the disclosure of PEYROVIAN does not remedy the deficiencies in the disclosures of BARHAM et al., YASUDA et al., and QUIGLEY et al. set forth above with respect to claim 24. Therefore, BARHAM et al., YASUDA et al., QUIGLEY et al., and PEYROVIAN, whether taken alone or in any reasonable combination, do not disclose or suggest the features recited in claims 34 and 35. For at least the foregoing reasons, Appellant submits that the rejection of claims 34 and 35 under 35 U.S.C. § 103(a) based on BARHAM et al., YASUDA et al., QUIGLEY et al., and PEYROVIAN is improper. Accordingly, Appellant requests that the rejection be reversed.

D. The rejection of claims 9, 10, 12, and 30-32 under 35 U.S.C. § 103(a) as unpatentable over BARHAM et al. in view of YASUDA et al., further in view of QUIGLEY et al., and still further in view of Appellant's Fig. 17(A) should be reversed.

1. Claims 9, 10, and 12

Claims 9, 10, and 12 depend from claim 1. Without acquiescing in the rejection of claims 9, 10, and 12, Appellant's Fig. 17(A) does not remedy the deficiencies in the disclosures of BARHAM et al., YASUDA et al., and QUIGLEY et al. set forth above with respect to claim 1. Therefore, BARHAM et al., YASUDA et al., QUIGLEY et al., and Appellant's Fig. 17(A), whether taken alone or in any reasonable combination, do not disclose or suggest the features recited in claims 9, 10, and 12. For at least the foregoing reasons, Appellant submits that the rejection of claims 9, 10, and 12 under 35 U.S.C. § 103(a) based on BARHAM et al., YASUDA et al., QUIGLEY et al., and Appellant's Fig., 17(A) is improper. Accordingly, Appellant requests that the rejection be reversed.

2. Claims 30-32

Claims 30-32 depend from claim 24. Without acquiescing in the rejection of claims 30-32, Appellant's Fig. 17(A) does not remedy the deficiencies in the disclosures of BARHAM et al., YASUDA et al., and QUIGLEY et al. set forth above with respect to claim 24. Therefore, BARHAM et al., YASUDA et al., QUIGLEY et al., and Appellant's Fig. 17(A), whether taken alone or in any reasonable combination, do not disclose or suggest the features recited in claims 30-32. For at least the foregoing reasons, Appellant submits that the rejection of claims 30-32 under 35 U.S.C. § 103(a) based on BARHAM et al., YASUDA et al., QUIGLEY et al., and Appellant's Fig., 17(A) is improper. Accordingly, Appellant requests that the rejection be reversed.

VIII. CONCLUSION

In view of the foregoing arguments, Appellant respectfully solicits the Honorable Board to reverse the Examiner's rejections of claims 1, 3-10, 12-17, and 22-40.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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IX. APPENDIX

1. A method for provisioning multiple digital receivers, comprising:

providing an analog to digital converter having an analog input and a digital output;

providing a plurality of digital receivers, each receiver having a programmable center frequency,

where the plurality of digital receivers are to receive digitized samples from the analog to digital converter and where each of the plurality of digital receivers includes a low-pass digital filter;

maintaining pre-computed sets of filter coefficients in non-volatile storage, each set corresponding to one of the plurality of low-pass digital filters, each filter having one of a predetermined set of bandwidths;

receiving a request to provision a selected one of the plurality of digital receivers;

selecting a first center frequency and a first bandpass bandwidth for provisioning the selected one of the plurality of digital receivers;

retrieving the filter coefficients associated with the first bandpass bandwidth;

subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency; and

loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers.

2. (canceled)

3. The method of claim 1, further including:

operating the selected one of the plurality of digital receivers at the first center

frequency;

subsequent to said operating, loading the coefficient latches in the selected one of the plurality of digital receivers with transformed coefficients corresponding to a second center frequency; and

operating the selected one of the plurality of digital receivers at the second center frequency.

4. The method of claim 3, further including:

selecting a third center frequency and a second bandpass bandwidth for provisioning a second one of the plurality of digital receivers, where said first and second bandpass bandwidths are unequal;

retrieving the filter coefficients associated with the third bandwidth;

subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the third center frequency; and

loading the transformed coefficients into coefficient latches in the second one of the plurality of digital receivers.

5. The method of claim 1, where the analog to digital converter and the plurality of digital receivers are located within the upstream section of a cable modem termination system (CMTS) channel bank organized into upstream and downstream channels.

6. The method of claim 5, where the ratio of the number of upstream channels demodulated by the CMTS channel bank to a number of upstream input connectors of the CMTS channel bank is M.

7. The method of claim 6, where M is 16.

8. The method of claim 1, where the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit.

9. The method of claim 5, where the CMTS channel bank is organized using a plurality of modules, each module having a plurality of downstream channels and a plurality of upstream channels.

10. The method of claim 9, where a number of the upstream channels is 4 times a number of the downstream channels.

11. (canceled)

12. The method of claim 5, where the CMTS channel bank has 4 times as many upstream channels as downstream channels.

13. The method of claim 5, where the CMTS is DOCSIS compatible.

14. The method of claim 5, where the upstream channels are in the 750-1000 MHz portion of the spectrum.

15. The method of claim 14, where at least one frequency stacker is used to densely pack

each sub-band of the 750-1000 MHz spectrum portion.

16. The method of claim 1, where each of the plurality of digital receivers includes a finite impulse response (FIR) digital filter.

17. The method of claim 16, where one or more of said FIR digital filters is an Optimum Equiripple Linear-Phase filter.

18-21. (canceled)

22. The method of claim 1, where a number of the filter coefficients for each of the low-pass digital filters is at least 16.

23. The method of claim 1, where a number of the filter coefficients for each of the low-pass digital filters is at most 24.

24. A system for provisioning multiple digital receivers, comprising:

an analog to digital converter having an analog input and a digital output;

a plurality of digital receivers, each of the plurality of digital receivers having a programmable center frequency, and each of the plurality of digital receivers including a low-pass digital filter;

means for coupling digitized samples to the plurality of digital receivers;

means for maintaining pre-computed sets of filter coefficients in non-volatile storage, each set corresponding to one of plurality of low-pass digital filters, each filter having one of a

predetermined set of bandwidths;

means for receiving a request to provision a selected one of the plurality of digital receivers;

means for selecting a first center frequency and a first bandpass bandwidth for provisioning the selected one of the plurality of digital receivers;

means for retrieving the filter coefficients associated with the first bandpass bandwidth;

means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the first center frequency; and

means for loading the transformed filter coefficients into coefficient latches in the selected one of the plurality of digital receivers.

25. The system of claim 24, further including:

means for operating the selected one of the plurality of digital receivers at the first center frequency;

means for loading, subsequent to said operating, the coefficient latches in the selected one of the plurality of digital receivers with transformed coefficients corresponding to a second center frequency; and

means for operating the selected one of the plurality of digital receivers at the second center frequency.

26. The system of claim 25, further including:

means for selecting a third center frequency and a second bandpass bandwidth for provisioning a second one of the plurality of digital receivers, where said first and second bandpass

bandwidths are unequal;

means for retrieving the filter coefficients associated with the third bandwidth;

means for subjecting the retrieved filter coefficients to a bandpass transformation corresponding to the third center frequency; and

means for loading the transformed coefficients into coefficient latches in the second one of the plurality of digital receivers.

27. The system of claim 24, where the analog to digital converter and the plurality of digital receivers are located within the upstream section of a CMTS channel bank organized into upstream and downstream channels.

28. The system of claim 27, where the ratio of the number of upstream channels demodulated by the CMTS channel bank to a number of upstream input connectors of the CMTS channel bank is M.

29. The system of claim 28, where M is 16.

30. The system of claim 27, where the CMTS channel bank is organized using a plurality of modules, each module having a plurality of downstream channels and a plurality of upstream channels.

31. The system of claim 30, where a number of the upstream channels is 4 times a number of the downstream channels.

32. The system of claim 27, where the CMTS channel bank has 4 times as many upstream channels as downstream channels.

33. The system of claim 27, where the CMTS is DOCSIS compatible.

34. The system of claim 27, where the upstream channels are in the 750-1000 MHz portion of the spectrum.

35. The system of claim 34, where at least one frequency stacker is used to densely pack each sub-band of the 750-1000 MHz spectrum portion.

36. The system of claim 24, where the analog to digital converter, the plurality of digital receivers, and the non-volatile storage are implemented on a single integrated circuit.

37. The system of claim 24, where each of the plurality of digital receivers includes a FIR digital filter.

38. The system of claim 37, where one or more of said FIR digital filters is an Optimum Equiripple Linear-Phase filter.

39. The system of claim 24, where a number of the filter coefficients for each filter is at least 16.

40. The system of claim 24, where a number of the filter coefficients for each filter is less

than or equal to 24.

X. EVIDENCE APPENDIX

None

XI. RELATED PROCEEDINGS APPENDIX

None